Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-30 (canceled)

31. (previously presented and indicated as allowable): An electronic access control device comprising:

a circuit having a portion deactivated during a first time period;

a portion of the circuit enabled during a second time period,

a portion of the circuit having an enable output signal generated in response to a sensed electromagnetic signal;

a portion of the circuit being enabled for an extended time period that is greater than the second time period;

a portion of the circuit having an input code output generated in response to an electromagnetic signal and during the extended time period;

a microprocessor having an unlock output signal generated if the input code matches the access code;

an electromechanical driver having an output signal generated in response to the unlock signal;

a non-volatile memory comprising a serial number; and,

a keypad operatively connected to the microprocessor for enabling a portion of the circuit and entering an access code.

32. (previously presented and indicated as allowable): An electronic access control device comprising:

a circuit having a portion deactivated during a first time period;

a portion of the circuit enabled during a second time period,

a portion of the circuit having an enable output signal generated in response to a sensed

electromagnetic signal;

a portion of the circuit being enabled for an extended time period that is greater than the second time period;

a portion of the circuit having an input code output generated in response to an electromagnetic signal and during the extended time period;

a microprocessor having an unlock output signal generated if the input code matches the access code;

an electromechanical driver having an output signal generated in response to the unlock signal;

a non-volatile memory comprising a serial number; and,

a program key operatively connected to the microprocessor for enabling a portion of the circuit and entering a program mode.

33. (previously presented and indicated as allowable): An electronic access control device comprising:

a circuit having a portion deactivated during a first time period;

a portion of the circuit enabled during a second time period,

a portion of the circuit having an enable output signal generated in response to a sensed electromagnetic signal;

a portion of the circuit being enabled for an extended time period that is greater than the second time period;

a portion of the circuit having an input code output generated in response to an electromagnetic signal and during the extended time period;

a microprocessor having an unlock output signal generated if the input code matches the access code;

an electromechanical driver having an output signal generated in response to the unlock signal; and,

a low-battery detection circuit enabled by the microprocessor for measuring a battery voltage, and wherein the low-battery detection circuit is disabled during the first time period and enabled during or after either the second or the extended time period.

34. (previously presented and indicated as allowable): An electronic access control device comprising:

a circuit having a portion deactivated during a first time period;

a portion of the circuit enabled during a second time period,

a portion of the circuit having an enable output signal generated in response to a sensed electromagnetic signal;

a portion of the circuit being enabled for an extended time period that is greater than the second time period;

a portion of the circuit having an input code output generated in response to an electromagnetic signal and during the extended time period;

a microprocessor having an unlock output signal generated if the input code matches the access code;

an electromechanical driver having an output signal generated in response to the unlock signal; and,

wherein the electromechanical driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state, and a signal for triggering a transition from the first state to the second state.

35. (previously presented and indicated as allowable): An electronic access control device comprising:

a circuit having a portion deactivated during a first time period;

a portion of the circuit enabled during a second time period,

a portion of the circuit having an enable output signal generated in response to a sensed electromagnetic signal;

a portion of the circuit being enabled for an extended time period that is greater than the second time period;

a portion of the circuit having an input code output generated in response to an electromagnetic signal and during the extended time period;

a microprocessor having an unlock output signal generated if the input code matches the access code;

an electromechanical driver having an output signal generated in response to the unlock signal;

a non-volatile memory comprising a serial number; and,

a communication port operatively connected to the microprocessor for sending the access code to the microprocessor that is written into a memory while the microprocessor is enabled, and the microprocessor entering a disabled mode sometime thereafter.

36. (previously presented and indicated as allowable): The device of claim 35 wherein the microprocessor is programmed to receive the serial number for the device through the communication port and write the serial number into the non-volatile memory when the processor is enabled, and the microprocessor is disabled sometime thereafter.

37. (previously presented and indicated as allowable): The device of claim 35 wherein the microprocessor transmits the serial number through the communication port to a device remote to the access control device when the processor is enabled, and the microprocessor is disabled sometime thereafter.

38. (canceled)

39. (canceled)

40. (previously presented and indicated as allowable): An apparatus comprising:

first circuit comprising an oscillator and having a first circuit output signal;

a second circuit temporarily enabled in response to the first circuit output signal, the second circuit having a second circuit output signal generated in response to receipt of an electromagnetic signal;

a third circuit temporarily enabled during the receipt of an electromagnetic signal, the circuit having a third circuit output signal comprising an input code generated in response to receipt of an electromagnetic signal;

a fourth circuit separate from and operatively coupled to the third circuit comprising a microprocessor temporarily enabled by the third circuit to compare the input code to an access code;

an electromechanical driver having an output that is provided to an unlock device if the input code matches the access code;

a non-volatile memory comprising a serial number; and,

a keypad operatively connected to the fourth circuit comprising a microprocessor for enabling the microprocessor and entering an access code.

41. (previously presented and indicated as allowable): An apparatus comprising:

a first circuit comprising an oscillator and having a first circuit output signal;

a second circuit temporarily enabled in response to the first circuit output signal, the second circuit having a second circuit output signal generated in response to receipt of an electromagnetic signal;

a third circuit temporarily enabled during the receipt of an electromagnetic signal, the circuit having a third circuit output signal comprising an input code generated in response to receipt of an electromagnetic signal;

a fourth circuit separate from and operatively coupled to the third circuit comprising a microprocessor temporarily enabled by the third circuit to compare the input code to an access code;

an electromechanical driver having an output that is provided to an unlock device if the input code matches the access code;

a non-volatile memory comprising a serial number; and,

the fourth circuit comprising a microprocessor and a program key operatively connected to the microprocessor for enabling the microprocessor to enter a program mode.

42. (previously presented and indicated as allowable): An apparatus comprising:

a first circuit comprising an oscillator and having a first circuit output signal;

a second circuit temporarily enabled in response to the first circuit output signal, the second circuit having a second circuit output signal generated in response to receipt of an electromagnetic signal;

a third circuit temporarily enabled during the receipt of an electromagnetic signal, the circuit having a third circuit output signal comprising an input code generated in response to receipt of an electromagnetic signal;

a fourth circuit separate from and operatively coupled to the third circuit comprising a microprocessor temporarily enabled by the third circuit to compare the input code to an access code;

an electromechanical driver having an output that is provided to an unlock device if the input code matches the access code; and,

the fourth circuit comprising a microprocessor and a low-battery detection circuit enabled by the microprocessor for measuring a battery voltage, and wherein the low-battery detection circuit is periodically disabled and enabled.

43. (previously presented and indicated as allowable): An apparatus comprising:

a first circuit comprising an oscillator and having a first circuit output signal;

a second circuit temporarily enabled in response to the first circuit output signal, the second circuit having a second circuit output signal generated in response to receipt of an electromagnetic signal;

a third circuit temporarily enabled during the receipt of an electromagnetic signal, the circuit having a third circuit output signal comprising an input code generated in response to receipt of an electromagnetic signal;

a fourth circuit separate from and operatively coupled to the third circuit comprising a microprocessor temporarily enabled by the third circuit to compare the input code to an access code;

an electromechanical driver having an output that is provided to an unlock device if the input code matches the access code; and,

the fourth circuit comprising a microprocessor and wherein the electromechanical driver has a first state and a second state, the driver output providing a lower non-zero power output in the second state than in the first state.

44. (previously presented and indicated as allowable): An apparatus comprising:

a first circuit comprising an oscillator and having a first circuit output signal;

a second circuit temporarily enabled in response to the first circuit output signal, the second circuit having a second circuit output signal generated in response to receipt of an electromagnetic signal;

a third circuit temporarily enabled during the receipt of an electromagnetic signal, the circuit having a third circuit output signal comprising an input code generated in response to receipt of an electromagnetic signal;

a fourth circuit separate from and operatively coupled to the third circuit comprising a microprocessor temporarily enabled by the third circuit to compare the input code to an access code;

an electromechanical driver having an output that is provided to an unlock device if the input code matches the access code;

a non-volatile memory comprising a serial number; and,

the fourth circuit comprising a microprocessor having a communication port for sending an access code to the microprocessor that is written into a memory when the microprocessor is enabled, and the processor is disabled sometime thereafter.

45. (previously presented and indicated as allowable): The apparatus of claim 44 wherein the microprocessor is programmed to receive a serial number through the communication port and write the serial number into the memory when the processor is enabled, and the processor is disabled sometime thereafter.

46. (previously presented and indicated as allowable): An apparatus comprising:

a first circuit comprising an oscillator and having a first circuit output signal;

a second circuit temporarily enabled in response to the first circuit output signal, the second circuit having a second circuit output signal generated in response to receipt of an electromagnetic signal;

a third circuit temporarily enabled during the receipt of an electromagnetic signal, the circuit having a third circuit output signal comprising an input code generated in response to receipt of an electromagnetic signal;

a fourth circuit separate from and operatively coupled to the third circuit comprising a microprocessor temporarily enabled by the third circuit to compare the input code to an access code;

an electromechanical driver having an output that is provided to an unlock device if the input code matches the access code;

the fourth circuit comprising a microprocessor having a communication port for sending an access code to the microprocessor that is written into a memory;

the microprocessor is programmed to receive a serial number through the communication port and write the serial number into the memory; and,

the microprocessor transmits the serial number through the communication port.

47. (canceled)

48. (canceled)

49. (previously presented and indicated as allowable): An apparatus comprising:

an oscillator having an output comprising a plurality of duty cycles;

a circuit that is periodically enabled for a time t_1 and disabled for a time t_2 during at least some of the duty cycles;

a portion of the circuit that generates an input code in response to an electromagnetic signal;

a microprocessor that is enabled and disabled and compares the input code to an access code when enabled;

a switch that upon sensing a signal of radio frequency enables the portion of the circuit as the input code is being received for a time t_3 that is greater than the time t_1;

a non-volatile memory comprising a serial number whereby the serial number is communicated by the microprocessor exclusively when enabled; and,

a keypad operatively connected to the microprocessor for enabling the microprocessor and entering an access code.

50. (previously presented and indicated as allowable): An apparatus comprising:

an oscillator having an output comprising a plurality of duty cycles;

a circuit that is periodically enabled for a time t_1 and disabled for a time t_2 during at least some of the duty cycles;

a portion of the circuit that generates an input code in response to an electromagnetic signal;

a microprocessor that is enabled and disabled and compares the input code to an access code when enabled;

a switch that upon sensing a signal of radio frequency, enables the portion of the circuit as the input code is being received for a time t_3 that is greater than the time t_1;

a non-volatile memory comprising a serial number whereby the serial number is communicated by the microprocessor exclusively when enabled; and,

a program key operatively connected to the microprocessor.

51. (previously presented and indicated as allowable): An apparatus comprising:

an oscillator having an output comprising a plurality of duty cycles;

a circuit that is periodically enabled for a time t_1 and disabled for a time t_2 during at least some of the duty cycles;

a portion of the circuit that generates an input code in response to an electromagnetic signal;

a microprocessor that compares the input code to an access code;

a switch that, upon sensing a signal of radio frequency, enables the portion of the circuit as the input code is being received for a time t_3 that is greater than the time t_1; and,

a low-battery detection circuit enabled by the microprocessor for measuring a battery voltage, and wherein the low-battery detection circuit is disabled during time t_2 and enabled either during or after either time t_1 or time t_3.

52. (previously presented and indicated as allowable): An apparatus comprising:

an oscillator having an output comprising a plurality of duty cycles;

a circuit that is periodically enabled for a time t_1 and disabled for a time t_2 during at least some of the duty cycles;

a portion of the circuit that generates an input code in response to an electromagnetic signal;

a microprocessor that compares the input code to an access code;

a switch that, upon sensing a signal of radio frequency, enables the portion of the circuit as the input code is being received for a time t_3 that is greater than the time t_1; and,

an electromechanical driver operatively connected to the microprocessor, the driver having a first state and a second state, and an output signal providing a lower non-zero power output in the second state than in the first state, and a timer for triggering a transition from the first state to the second state.

53. (previously presented and indicated as allowable): An apparatus comprising:

an oscillator having an output comprising a plurality of duty cycles;

a circuit that is periodically enabled for a time t_1 and disabled for a time t_2 during at least some of the duty cycles;

a portion of the circuit that generates an input code in response to an electromagnetic signal;

a microprocessor that is enabled and disabled and compares the input code to an access code when enabled;

a switch that, upon sensing a signal of radio frequency, enables the portion of the circuit as the input code is being received for a time t_3 that is greater than the time t_1;

a non-volatile memory comprising a serial number whereby the serial number is communicated by the microprocessor exclusively when enabled; and,

a communication port operatively connected to the microprocessor for sending the access code to the microprocessor that is written into a memory when the microprocessor is enabled, and the microprocessor entering a disabled mode sometime thereafter.

54. (previously presented and indicated as allowable): The device of claim 53 wherein the microprocessor is programmed to receive a serial number for the device through the communication port and write the serial number into the memory when the processor is enabled, and the processor is disabled sometime thereafter.

55. (previously presented and indicated as allowable): The device of claim 53 wherein the microprocessor transmits the serial number through the communication port when the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

56. (canceled)

57. (canceled)

58. (previously presented and indicated as allowable): A circuit operating on current drained from a battery comprising:

a timer enabled electronic circuit for sensing a signal of radio frequency having an output that indicates detection of a device capable of providing an electromagnetic signal;

a decoder that extracts an input code transmitted via the electromagnetic signal;

a switch that, in response to an input, increases the current drained from the battery;

an electronic circuit that compares the input code to an access code;

an electronic circuit that provides an output to an unlock device if the input code matches the access code;

wherein the switch decreases the current drained from the battery after receiving the input code;

a non-volatile memory comprising a serial number and a microprocessor that is enabled and disabled whereby the serial number is communicated by the microprocessor exclusively when enabled; and,

a keypad operatively connected to the comparing circuit comprising a microprocessor for enabling a circuit and entering an access code.

59. (previously presented and indicated as allowable): A circuit operating on current drained from a battery comprising:

a timer enabled electronic circuit for sensing a signal of radio frequency having an output that indicates detection of a device capable of providing an electromagnetic signal;

a decoder that extracts an input code transmitted via the electromagnetic signal;

a switch that, in response to an input, increases the current drained from the battery;

an electronic circuit that compares the input code to an access code;

an electronic circuit that provides an output to an unlock device if the input code matches the access code, wherein the switch decreases the current drained from the battery after receiving the input code;

a non-volatile memory comprising a serial number and a microprocessor that is enabled and disabled whereby the serial number is communicated by the microprocessor exclusively when enabled; and,

the comparing circuit comprising a microprocessor and a program key operatively connected to the microprocessor for enabling a circuit to enter a program mode.

60. (previously presented and indicated as allowable): A circuit operating on current drained from a battery comprising:

a timer enabled electronic circuit for sensing a signal of radio frequency having an output that indicates detection of a device capable of providing an electromagnetic signal;

a decoder that extracts an input code transmitted via the electromagnetic signal;

a switch that, in response to an input, increases the current drained from the battery;

an electronic circuit that compares the input code to an access code;

an electronic circuit that provides an output to an unlock device if the input code matches the access code;

wherein the switch decreases the current drained from the battery after receiving the input code; and,

the comparing circuit comprising a microprocessor and a low-battery detection circuit enabled by the microprocessor for measuring a voltage associated with the battery, and wherein the low-battery detection circuit is periodically disabled and enabled.

61. (previously presented and indicated as allowable): A circuit operating on current drained from a battery comprising:

a timer enabled electronic circuit for sensing a signal of radio frequency having an output that indicates detection of a device capable of providing an electromagnetic signal;

a decoder that extracts an input code transmitted via the electromagnetic signal;

a switch that, in response to an input, increases the current drained from the battery;

an electronic circuit that compares the input code to an access code;

an electronic circuit that provides an output to an unlock device if the input code matches the access code;

wherein the switch decreases the current drained from the battery after receiving the input code; and,

the comparing circuit comprising a microprocessor and wherein the circuit providing the output to the unlock device comprising an electromechanical driver having a first state and a second state, the driver output providing a lower non-zero power output in the second state than in the first state, and a signal for triggering a transition from the first state to the second state.

62. (previously presented and indicated as allowable): A circuit operating on current drained from a battery comprising:

a timer enabled electronic circuit for sensing a signal of radio frequency having an output that indicates detection of a device capable of providing an electromagnetic signal;

a decoder that extracts an input code transmitted via the electromagnetic signal;

a switch that, in response to an input, increases the current drained from the battery;

an electronic circuit that compares the input code to an access code;

an electronic circuit that provides an output to an unlock device if the input code matches the access code;

wherein the switch decreases the current drained from the battery after receiving the input code;

the comparing circuit comprising a microprocessor having a communication port for sending the access code to the microprocessor that is written into a memory while the microprocessor is enabled, and the microprocessor is disabled sometime thereafter; and,

a non-volatile memory comprising a serial number whereby the serial number is communicated by the microprocessor exclusively when enabled.

63. (previously presented and indicated as allowable): The circuit of claim 62 wherein the microprocessor is programmed to receive a serial number through the communication port and write the serial number into the memory while the microprocessor is enabled, and the processor is disabled sometime thereafter.

64. (previously presented and indicated as allowable): The circuit of claim 63 wherein the microprocessor transmits the serial number through the communication port while the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

65. (canceled)

66. (previously presented and indicated as allowable): The electronic access control device of claim 31, wherein the circuit draws less than 100 micro-amps from a battery during the first time period and draws greater than 100 micro-amps from a battery during the extended time period.

67. (previously presented and indicated as allowable): The electronic access control device of claim 31, wherein a memory contains a value separate from the access code for limiting access of the device.

68. (previously presented and indicated as allowable): The electronic access control device of claim 31, further comprising a communication port operatively connected to a processor for receiving a code while the processor is enabled that is stored into a memory, said code sent from a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

69. (previously presented and indicated as allowable): The electronic access control device of claim 31, further comprising a communication port operatively connected to a processor, and

wherein the processor is programmed to transmit an access code stored in a memory through the communication port while the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

70. (previously presented and indicated as allowable): The electronic access control device of claim 31, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit the serial number stored in a memory through the communication port while the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

71. (currently amended): The electronic access control device of claim 31 further comprising a low-battery detection circuit occasionally disabled and being initiated ~~enabled~~ by the microprocessor for measuring a battery voltage when the microprocessor is enabled~~, and wherein the low-battery detection circuit is disabled during the first time period and enabled during or after the extended time period~~.

72. (previously presented and indicated as allowable): The electronic access control device of claim 31 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

73. (previously presented and indicated as allowable): The electronic access control device of claim 31, wherein the access code received by the keypad is stored in a memory.

74. (previously presented and indicated as allowable): The electronic access control device of claim 31, further comprising a program key wherein the program key is pressed prior to storing an access code in a memory.

75. (previously presented and indicated as allowable): The electronic access control device of claim 31, wherein the keypad receives an access code which is compared to an access code stored in a memory.

76. (previously presented and indicated as allowable): The electronic access control device of claim 31, wherein a circuit generates an enable signal in response to pressing a first key on a keypad used in entering an input code, the input code comprising the first key and at least one subsequent keypad entry.

77. (cancel):

78. (previously presented and indicated as allowable): The electronic access control device of claim 33, wherein the circuit draws less than 100 micro-amps from a battery during the first time period and draws greater than 100 micro-amps from a battery during the extended time period.

79. (previously presented and indicated as allowable): The electronic access control device of claim 33, wherein a memory contains a value separate from the access code for limiting access of the device.

80. (previously presented and indicated as allowable): The electronic access control device of claim 33, further comprising a communication port operatively connected to a processor for sending a code to the processor while the processor is enabled that is stored into a memory sent from a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

81. (previously presented and indicated as allowable): The electronic access control device of claim 33, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit an access code stored in a memory through the

communication port while the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

82. (previously presented and indicated as allowable): The electronic access control device of claim 33, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to communicate the serial number through the communication port while the processor is enabled with a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

83. (previously presented and indicated as allowable): The electronic access control device of claim 33 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

84. (previously presented and indicated as allowable): The electronic access control device of claim 33, further comprising a program key wherein the program key is pressed prior to storing the access code in a memory.

85. (previously presented and indicated as allowable): The electronic access control device of claim 33, further comprising a keypad wherein the keypad receives an access code which is compared to an access code stored in a memory.

86. (previously presented and indicated as allowable): The electronic access control device of claim 33, further comprising a keypad wherein a circuit generates a wake-up signal in response to pressing a first key on a keypad used in entering an input code comprising the first key and at least one subsequent keypad entry.

87. (cancel):

88. (previously presented and indicated as allowable): The electronic access control device of claim 35, wherein the circuit draws less than 100 micro-amps from a battery during the first time period and draws greater than 100 micro-amps from a battery during the extended time period.

89. (previously presented and indicated as allowable): The electronic access control device of claim 35, wherein a memory contains a value separate from the access code for limiting access of the device.

90. (previously presented and indicated as allowable): The electronic access control device of claim 35, wherein the processor is programmed to transmit an access code stored in a memory through the communication port while the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

91. (previously presented and indicated as allowable): The electronic access control device of claim 35, wherein the processor is programmed to transmit a serial number stored in a memory through the communication port while the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

92. (previously presented and indicated as allowable): The electronic access control device of claim 35 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

93. (previously presented and indicated as allowable): The electronic access control device of claim 35, further comprising a program key wherein the program key is pressed prior to storing the access code in a memory.

94. (previously presented and indicated as allowable): The electronic access control device of claim 35, further comprising a keypad wherein the keypad receives an access code which is compared to an access code stored in a memory.

95. (previously presented and indicated as allowable): The electronic access control device of claim 35, further comprising a keypad wherein a circuit generates a wake-up signal in response to pressing a first key on a keypad used in entering an input code comprising the first key and at least one subsequent keypad entry.

96. (cancel):

97. (previously presented and indicated as allowable): The apparatus of claim 49, wherein the circuit draws less than 100 micro-amps from a battery during time t_2 and draws greater than 100 micro-amps from a battery during time t_3.

98. (previously presented and indicated as allowable): The apparatus of claim 49, wherein a memory contains a limit value separate from the access code for limiting the output to the lock device.

99. (previously presented and indicated as allowable): The apparatus of claim 49, further comprising a communication port operatively connected to a processor for sending a code to the processor that is stored into a memory sent from a device remote to the apparatus.

100. (previously presented and indicated as allowable): The apparatus of claim 49, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit an access code stored in a memory through the communication port to a device remote to the apparatus.

101. (previously presented and indicated as allowable): The apparatus of claim 49, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit a serial number stored in a memory through the communication port to a device remote to the apparatus.

102. (currently amended): The apparatus of claim 49 further comprising a low-battery detection circuit occasionally disabled and being initiated ~~enabled~~ by the microprocessor for measuring a battery voltage when the microprocessor is enabled~~, and wherein the low-battery detection circuit is disabled during time t_2 and enabled during or after time t_3~~.

103. (previously presented and indicated as allowable): The apparatus of claim 49 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

104. (previously presented and indicated as allowable): The apparatus of claim 49, wherein the keypad receives an access code which is stored in a memory.

105. (previously presented and indicated as allowable): The apparatus of claim 49, further comprising a program key wherein the program key is pressed prior to storing an access code in a memory.

106. (previously presented and indicated as allowable): The apparatus of claim 49, wherein the keypad receives an access code which is compared to an access code stored in a memory.

107. (previously presented and indicated as allowable): The apparatus of claim 49, wherein a circuit generates a wake-up signal in response to pressing a key on the keypad.

108. (previously presented and indicated as allowable): The apparatus of claim 49, wherein a circuit generates a wake-up signal in response to pressing a first key on a keypad used in entering an input code comprising the first key and at least one subsequent keypad entry.

109. (canceled):

110. (previously presented and indicated as allowable): The apparatus of claim 51, wherein the circuit draws less than 100 micro-amps from a battery during time t_2 and draws greater than 100 micro-amps from a battery during time t_3.

111. (previously presented and indicated as allowable): The apparatus of claim 51, wherein a memory contains a limit value separate from the access code for limiting the output to the lock device.

112. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising a communication port operatively connected to a processor for sending a code to the processor that is stored into a memory sent from a device remote to the apparatus.

113. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit an access code stored in a memory through the communication port to an apparatus remote to the apparatus.

114. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to communicate a serial number through the communication port with a device remote to the apparatus while the processor is enabled, and the processor is disabled sometime thereafter.

115. (previously presented and indicated as allowable): The apparatus of claim 51 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

116. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising a program key wherein the program key is pressed prior to storing the access code in a memory.

117. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising a keypad wherein the keypad receives an access code which is compared to an access code stored in a memory.

118. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising a keypad wherein a circuit generates a wake-up signal in response to pressing a first key on a keypad used in entering an input code comprising the first key and at least one subsequent keypad entry.

119. (cancel):

120. (previously presented and indicated as allowable): The apparatus of claim 53, wherein the circuit draws less than 100 micro-amps from a battery during time t_2 and draws greater than 100 micro-amps from a battery during time t_3.

121. (previously presented and indicated as allowable): The apparatus of claim 53, wherein a memory contains a limit value separate from the access code for limiting the output to the lock device.

122. (previously presented and indicated as allowable): The apparatus of claim 53, wherein the processor is programmed to transmit an access code stored in a memory through the communication port to a device remote to the apparatus.

123. (cancel):

124. (previously presented and indicated as allowable): The apparatus of claim 53 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

125. (previously presented and indicated as allowable): The apparatus of claim 53, further comprising a program key wherein the program key is pressed prior to storing the access code in a memory.

126. (previously presented and indicated as allowable): The apparatus of claim 53, further comprising a keypad wherein the keypad receives an access code which is compared to an access code stored in a memory.

127. (previously presented and indicated as allowable): The apparatus of claim 53, further comprising a keypad wherein a circuit generates a wake-up signal in response to pressing a first key on a keypad used in entering an input code comprising the first key and at least one subsequent keypad entry.

128. (cancel):

129. (previously presented and indicated as allowable): The circuit of claim 58, wherein the circuit draws less than 100 micro-amps from the battery before the switch activates and draws greater than 100 micro-amps from the battery after the switch activates.

130. (previously presented and indicated as allowable): The circuit of claim 58, wherein a memory contains a value separate from the access code for limiting the output to the lock device.

131. (previously presented and indicated as allowable): The circuit of claim 58, further comprising a communication port operatively connected to a processor for sending a code to the processor while the processor is enabled that is stored into a memory sent from a device remote to the circuit, and the processor is disabled sometime thereafter.

132. (previously presented and indicated as allowable): The circuit of claim 58, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit an access code stored in a memory through the communication port while the processor is enabled to a device remote to the circuit, and the processor is disabled sometime thereafter.

133. (previously presented and indicated as allowable): The circuit of claim 58, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit a serial number stored in a memory through the communication port while the processor is enabled to a device remote to the circuit, and the processor is disabled sometime thereafter.

134. (currently amended): The circuit of claim 58 further comprising a low-battery detection circuit occasionally disabled and being initiated ~~enabled~~ by the microprocessor for measuring a battery voltage~~, and wherein the low-battery detection circuit is disabled while the microprocessor is disabled and enabled~~ while the microprocessor is enabled.

135. (previously presented and indicated as allowable): The circuit of claim 58 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

136. (previously presented and indicated as allowable): The circuit of claim 134, further comprising a communication port operatively connected to a processor for sending a code to the processor while the processor is enabled that is stored into a memory sent from a device remote to the circuit, and the processor is disabled sometime thereafter.

137. (previously presented and indicated as allowable): The circuit of claim 58, further comprising a program key wherein the program key is pressed prior to storing an access code in a memory.

138. (previously presented and indicated as allowable): The circuit of claim 136, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit an access code stored in a memory through the communication port while the processor is enabled to a device remote to the circuit, and the processor is disabled sometime thereafter.

139. (previously presented and indicated as allowable): The circuit of claim 58, wherein a circuit generates a wake-up signal in response to pressing a key on the keypad.

140. (previously presented and indicated as allowable): The circuit of claim 58, wherein a circuit generates a wake-up signal in response to pressing a first key on a keypad used in entering an input code comprising the first key and at least one subsequent keypad entry.

141. (cancel):

142. (previously presented and indicated as allowable): The circuit of claim 60, wherein a serial number is stored in a non-volatile memory.

143. (previously presented and indicated as allowable): The circuit of claim 60, wherein a memory contains a value separate from the access code for limiting the output to the unlock device.

144. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising a communication port operatively connected to a processor for sending a code to the processor while the processor is enabled that is stored into a memory sent from a device remote to the apparatus ~~circuit~~, and the processor is disabled sometime thereafter.

145. (previously presented and indicated as allowable): The circuit of claim 60, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit an access code stored in a memory through the communication port while the processor is enabled to a device remote to the circuit, and the processor is disabled sometime thereafter.

146. (previously presented and indicated as allowable): The circuit of claim 60, further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to communicate a serial number through the communication port while the processor is enabled with a device remote to the circuit, and the processor is disabled sometime thereafter.

147. (previously presented and indicated as allowable): The circuit of claim 60 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

148. (previously presented and indicated as allowable): The circuit of claim 60, further comprising a program key wherein the program key is pressed prior to storing the access code in a memory.

149. (previously presented and indicated as allowable): The circuit of claim 60, further comprising a keypad wherein the keypad receives an access code which is compared to an access code stored in a memory.

150. (previously presented and indicated as allowable): The circuit of claim 60, further comprising a keypad wherein a circuit generates a wake-up signal in response to pressing a first key on a keypad used in entering an input code comprising the first key and at least one subsequent keypad entry.

151. (cancel):

152. (previously presented and indicated as allowable): The circuit of claim 62, wherein the current drained from the battery is less than 100 micro-amps before the switch activates and the current drained from the battery is greater than 100 micro-amps after the switch activates.

153. (currently amended): The circuit of claim 152 further comprising a low-battery detection circuit occasionally disabled and being initiated ~~enabled~~ by the microprocessor for measuring a battery voltage~~, and wherein the low-battery detection circuit is disabled while the microprocessor is disabled and enabled~~ while the microprocessor is enabled.

154. (previously presented and indicated as allowable): The circuit of claim 153 further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to transmit an access code stored in a memory through the communication port while the processor is enabled to a device remote to the circuit, and the processor is disabled sometime thereafter.

155. (previously presented and indicated as allowable): The circuit of claim 154 further comprising a communication port operatively connected to a processor, and wherein the processor is programmed to communicate a serial number through the communication port while

the processor is enabled with a device remote to the circuit, and the processor is disabled sometime thereafter.

156. (previously presented and indicated as allowable): The circuit of claim 155 wherein a memory contains a limit value separate from the access code for limiting the output to the lock device.

157. (previously presented and indicated as allowable): The circuit of claim 156 further comprising a keypad wherein the keypad receives an access code which is compared to an access code stored in a memory.

158. (previously presented and indicated as allowable): The circuit of claim 62, wherein a memory contains a value separate from the access code that limits the output to the unlock device.

159. (previously presented and indicated as allowable): The circuit of claim 62, wherein the processor is programmed to transmit an access code stored in a memory through the communication port to a device remote to the circuit.

160. (previously presented and indicated as allowable): The circuit of claim 62, wherein the processor is programmed to transmit a serial number stored in a memory through the communication port to a device remote to the circuit.

161. (previously presented and indicated as allowable): The circuit of claim 62 wherein the driver has a first state and a second state, the driver output signal providing a lower non-zero power output in the second state than in the first state.

162. (previously presented and indicated as allowable): The circuit of claim 62, further comprising a program key wherein the program key is pressed prior to storing the access code in a memory.

163. (previously presented and indicated as allowable): The circuit of claim 62, further comprising a keypad wherein the keypad receives an access code which is compared to an access code stored in a memory.

164. (previously presented and indicated as allowable): The circuit of claim 62, further comprising a keypad wherein a circuit generates a wake-up signal in response to pressing a first key on a keypad used in entering an input code comprising the first key and at least one subsequent keypad entry.

165. (cancel):

166. (previously presented and indicated as allowable): The circuit of claim 62 wherein at least a portion of the circuit is periodically disabled by a timer or an oscillator.

167. (currently amended): The circuit of claim 166 further comprising a low-battery detection circuit occasionally disabled and being initiated ~~enabled~~ by the microprocessor for measuring a battery voltage~~, and wherein the low-battery detection circuit is disabled while the microprocessor is disabled and enabled~~ while the microprocessor is enabled.

168. (currently amended): The apparatus of claim 44 further comprising a low-battery detection circuit occasionally disabled and being initiated ~~enabled~~ by a microprocessor for measuring a battery voltage~~, and wherein the low-battery detection circuit is disabled while the microprocessor is disabled and enabled~~ while the microprocessor is enabled.

169. (previously presented and indicated as allowable): The apparatus of claim 168, further comprising a communication port operatively connected to a processor, and wherein the

processor is programmed to transmit an access code and a serial number stored in a memory through the communication port to a device remote to the apparatus.

170. (previously presented and indicated as allowable): The circuit of claim 58, wherein the keypad receives an access code which is stored in a memory.

171. (previously presented and indicated as allowable): The circuit of claim 58, wherein the keypad receives an access code which is compared to an access code stored in a memory.

172. (previously presented and indicated as allowable): The access control device of claim 33, comprising two processors, a first processor is the microprocessor having an unlock output signal generated if the input code matches the access code and is shielded from external access, and a second processor obtains the input code and communicates the input code to the first processor.

173. (previously presented and indicated as allowable): The circuit of claim 172 further comprising a communication port operatively connected to one of the processors, and wherein said processor is programmed to receive an access code through the communication port and store the access code in a memory while said processor is enabled, and said processor is disabled sometime thereafter.

174. (previously presented and indicated as allowable): The circuit of claim 173, wherein the first or second processor is programmed to communicate a serial number through the communication port while the said processor is enabled with a device remote to the circuit, and said processor is disabled sometime thereafter.

175. (previously presented and indicated as allowable): The circuit of claim 174, further comprising a communication port operatively connected to the first or second processor, and wherein said processor is programmed to transmit an access code stored in a memory through the

communication port while said processor is enabled to a device remote to the circuit, and said processor is disabled sometime thereafter.

176. (previously presented and indicated as allowable): The circuit of claim 175, wherein the current drained from the battery is less than 100 micro-amps during the first time period and the current drained from the battery is greater than 100 micro-amps during the extended time period.

177. (previously presented and indicated as allowable): The circuit of claim 176, wherein a memory contains a limit value separate from the access code for limiting the unlock signal.

178. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising two processors, wherein a first processor is the microprocessor for comparing the input code with the access code and is shielded from external access and a second processor obtains the input code and communicates the input code to the first processor.

179. (previously presented and indicated as allowable): The circuit of claim 178, wherein the first or second processor is programmed to communicate a serial number through the communication port while the microprocessor is enabled with a device remote to the circuit, and the microprocessor is disabled sometime thereafter.

180. (previously presented and indicated as allowable): The circuit of claim 179, further comprising a communication port operatively connected to one of the processors, and wherein at least one of the first and second processors is programmed to transmit an access code stored in a memory through the communication port while at least one of the first and second processors is enabled to a device remote to the circuit, and at least one of the first and second processors is disabled sometime thereafter.

181. (previously presented and indicated as allowable): The circuit of claim 180, wherein the current drained from the battery is less than 100 micro-amps during time t_2 and the current drained from the battery is greater than 100 micro-amps during time t_3.

182. (previously presented and indicated as allowable): The circuit of claim 181, wherein a memory contains a limit value separate from the access code for limiting the output to the lock device.

183. (previously presented and indicated as allowable): The apparatus of claim 110, further comprising a communication port operatively connected to the processor, and wherein the microprocessor is programmed to transmit an access code stored in a memory through the communication port while the microprocessor is enabled to a device remote to the circuit, and the microprocessor is disabled sometime thereafter.

184. (previously presented and indicated as allowable): The apparatus of claim 183, wherein the microprocessor is programmed to communicate a serial number through the communication port with a device remote to the apparatus while the microprocessor is enabled, and the microprocessor is disabled sometime thereafter.

185. (previously presented and indicated as allowable): The apparatus of claim 184, further comprising a communication port operatively connected to the microprocessor for receiving a code while the processor is enabled that is stored into a memory, said code sent from a device remote to the electronic access control device, and the microprocessor is disabled sometime thereafter.

186. (previously presented and indicated as allowable): The apparatus of claim 51, further comprising a communication port operatively connected to the microprocessor, and wherein the microprocessor is programmed to transmit an access code stored in a memory through the

communication port while the microprocessor is enabled to a device remote to the circuit, and the microprocessor is disabled sometime thereafter.

187. (previously presented and indicated as allowable): The apparatus of claim 186, further comprising a communication port operatively connected to a microprocessor for receiving a code while the microprocessor is enabled that is stored into a memory, said code sent from a device remote to the electronic access control device, and the microprocessor is disabled sometime thereafter.

188. (previously presented and indicated as allowable): The apparatus of claim 187, wherein the microprocessor is programmed to communicate a serial number through the communication port with a device remote to the apparatus.

189. (previously presented and indicated as allowable): The apparatus of claim 188, wherein the current drained from the battery is less than 100 micro-amps during time t_1 and the current drained from the battery is greater than 100 micro-amps during time t_3.

190. (previously presented and indicated as allowable): The apparatus of claim 188, wherein a memory contains a limit value separate from the access code for limiting the output to the lock device.

191. (previously presented and indicated as allowable): The apparatus of claim 188, further comprising a program key wherein the program key is pressed prior to storing the access code in a memory.

192. (previously presented and indicated as allowable): The apparatus of claim 188, further comprising a keypad wherein the keypad receives an access code which is compared to an access code stored in a memory.

193. (previously presented and indicated as allowable): The apparatus of claim 188, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

194. (previously presented and indicated as allowable): The apparatus of claim 49, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

195. (previously presented and indicated as allowable): The apparatus of claim 51, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

196. (previously presented and indicated as allowable): The apparatus of claim 53, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

197. (previously presented and indicated as allowable): The apparatus of claim 33, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

198. (previously presented and indicated as allowable): The circuit of claim 62, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

199. (previously presented and indicated as allowable): The circuit of claim 64, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

200. (previously presented and indicated as allowable): The circuit of claim 172, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

201. (previously presented and indicated as allowable): An access control system for accessing an enclosure or a secure area by energizing a lock actuator, the access control system comprising:

a first processor circuit comprising:

a first processor having one or more activated modes and a deactivated mode of operation, the deactivated mode of operation requiring less power than an activated mode of operation;

a memory comprising a time and/or date value;

a sensing circuit for sensing a wake up signal;

a circuit for obtaining an input code; and,

a communication port configured to communicate: (i) a serial number; (ii) the input code; and, (iii) the time and/or date value while the first processor is in an activated mode;

a second processor circuit comprising:

a second processor separated from the first processor;

a memory having stored therein at least one access code and a serial number; and,

a communication port configured for communication of:

the input code;

and the serial number; and,

wherein the first processor is configured to be activated in response to a wake up signal sensed by the sensing circuit and to communicate the input code to the second processor, the second processor being configured to have an unlock output signal generated if the input code matches the access code;

an electromechanical driver and a battery for energizing a lock actuator in response to receiving an unlock output signal, the driver having a first state and a second state and the unlock output signal providing for a lower, non-zero, power output to the actuator in the second

state than in the first state; and,

a low voltage detection circuit for measuring a voltage of the battery, the low voltage detection circuit only being enabled for measurement during a period of time when the first processor is in an activated mode.

202. (previously presented and indicated as allowable): The access control system of claim 201, wherein the communication port of the second processor configured for communication of the time and/or date value.

203. (previously presented and indicated as allowable): The access control system of claim 201, wherein a limit value is communicated with a device external to the access control system.

204. (previously presented and indicated as allowable): The access control system of claim 201, wherein the serial number is communicated between the first processor and second processor.

205. (previously presented and indicated as allowable): The access control system of claim 201, where the serial number is communicated with a device external to the access control system.

206. (previously presented and indicated as allowable): The circuit of claim 201, wherein the driver is controlled by a timer.

207. (previously presented and indicated as allowable): The circuit of claim 201, wherein the current drained from the battery is less than 100 micro-amps during a time the first processor is deactivated and the current drained from the battery is greater than 100 micro-amps during a time the first processor is activated.

208. (previously presented and indicated as allowable): The access control system of claim 201, wherein the input code is communicated with a device external to the access control system.

209. (previously presented and indicated as allowable): The access control system of claim 201, wherein the input code or the serial number communicated between the first processor and second processor is encrypted.

210. (previously presented and indicated as allowable): A battery powered access control system for accessing an enclosure or a secure area by energizing a lock actuator, the access control system including a first and a second processors and further comprising:

an oscillator or timer having an output comprising a plurality of duty cycles;

a circuit that is periodically enabled for a time t_1 and disabled for a time t_2 during at least some of the duty cycles;

a portion of the circuit that generates an input code in response to an electromagnetic signal;

a first processor that compares the input code to an access code;

a switch that, upon sensing an electromagnetic signal, enables the portion of the circuit as the input code is being received for a time t_3 that is greater than the time t_1; and,

an electromechanical driver operatively connected to the first processor, the driver having a first state and a second state, and an output signal providing a lower non-zero power output in the second state than in the first state;

a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled;

a memory comprising a time and/or date value and a serial number; and,

a communication port operatively connected to the first processor configured to communicate the serial number, the access code and the time and/or date value between the first and second processors while the second processor is activated, and the second processor is deactivated sometime thereafter.

211. (previously presented and indicated as allowable): The access control system of claim 210, wherein the time and/or date value is communicated with a device external to the access control system.

212. (previously presented and indicated as allowable): The access control system of claim 210, wherein a limit value is communicated with a device external to the access control system.

213. (previously presented and indicated as allowable): The access control system of claim 210, wherein the input code is communicated with a device external to the access control system.

214. (previously presented and indicated as allowable): The access control system of claim 210, wherein the serial number is communicated with a device external to the access control system.

215. (previously presented and indicated as allowable): The access control system of claim 210, further comprising a timer for triggering a transition of the electromechanical driver from the first state to the second state.

216. (previously presented and indicated as allowable): The access control system of claim 210, wherein the input code or the serial number communicated between the first processor and second processor is encrypted.

217. (previously presented and indicated as allowable): The access control system of claim 210, wherein the current drained from the battery is less than 100 micro-amps during a time the first processor is deactivated and the current drained from the battery is greater than 100 micro-amps during a time the first processor is activated.

218. (currently amendment): The access control system of claim 248, [[~~35,~~]] further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

219. (previously presented and indicated as allowable): The apparatus of claim 44, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

220. (previously presented and indicated as allowable): The apparatus of claim 46, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

221. (previously presented and indicated as allowable): The apparatus of claim 53, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

222. (previously presented and indicated as allowable): The circuit of claim 62, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

223. (currently amendment): The access control system of claim 227, [[~~34,~~]] further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

224. (previously presented and indicated as allowable): The apparatus of claim 43, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

225. (previously presented and indicated as allowable): The apparatus of claim 52, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

226. (previously presented and indicated as allowable): The circuit of claim 61, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is temporarily enabled and disabled.

227. (new): The access control device of claim 34 wherein the device comprises two processors, a first processor is the microprocessor having an unlock output signal generated if the input code matches the access code, and a second processor obtains the input code and communicates the input code to the first processor.

228. (new): The electronic access control device of claim 227, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the access control device.

229. (new): The electronic access control device of claim 227, wherein the input code or a serial number communicated between the first processor and second processor is encrypted.

230. (new): The electronic access control device of claim 227, wherein the circuit draws less than 100 micro-amps from a battery during the first time period and draws greater than 100 micro-amps from a battery during the extended time period.

231. (new): The electronic access control device of claim 227, wherein a memory contains a value separate from the access code for limiting access of the device.

232. (new): The electronic access control device of claim 227, wherein one of the processors is programmed to transmit a serial number stored in a memory through the communication port

while the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

233. (new): The electronic access control device of claim 227, further comprising a communication port operatively connected to one of the processors for sending a code to the processor while the processor is enabled that is stored into a memory sent from a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

234. (new): The electronic access control device of claim 232, further comprising a communication port operatively connected to a processor for sending a code to the processor while the processor is enabled that is stored into a memory sent from a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

235. (new): The electronic access control device of claim 234, wherein a memory contains a value separate from the access code for limiting access of the device.

236. (new): The electronic access control device of claim 235, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the access control device.

237. (new): The electronic access control device of claim 236, wherein the input code or a serial number communicated between the first processor and second processor is encrypted.

238. (new): The electronic access control device of claim 237, wherein the circuit draws less than 100 micro-amps from a battery during the first time period and draws greater than 100 micro-amps from a battery during the extended time period.

239. (new): The apparatus of claim 43, wherein the circuit draws less than 100 micro-amps from a battery during a disabled time period and draws greater than 100 micro-amps from a battery during the enabled time period.

240. (new): The apparatus of claim 43, wherein a memory contains a value separate from the access code for limiting access of the apparatus.

241. (new): The apparatus of claim 43, wherein a processor is programmed to transmit a serial number stored in a memory through the communication port while the processor is enabled to a device remote to the apparatus, and the processor is disabled sometime thereafter.

242. (new): The apparatus of claim 43, further comprising a communication port operatively connected to a processor for sending a code to the processor while the processor is enabled that is stored into a memory sent from a device remote to the apparatus, and the processor is disabled sometime thereafter.

243. (new): The apparatus of claim 43, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

244. (new): The apparatus of claim 43, wherein the input code or a serial number communicated by a processor is encrypted.

245. (new): The apparatus of claim 240, further comprising a communication port operatively connected to a processor for sending a code to the processor while the processor is enabled that is stored into a memory sent from a device remote to the apparatus, and the processor is disabled sometime thereafter.

246. (new): The apparatus of claim 245, wherein a memory contains a value separate from the access code for limiting access of the apparatus.

247. (new): The apparatus of claim 246, wherein the circuit draws less than 100 micro-amps from a battery during a disabled time period and draws greater than 100 micro-amps from a battery during the enabled time period.

248. (new): The electronic access control device of claim 35, comprising two processors, a first processor is the microprocessor having an unlock output signal generated if the input code matches the access code, and a second processor obtains the input code and communicates the input code to the first processor.

249. (new): The electronic access control device of claim 248, wherein a memory contains a value separate from the access code for limiting access of the device.

250. (new): The electronic access control device of claim 248, wherein the circuit draws less than 100 micro-amps from a battery during the first time period and draws greater than 100 micro-amps from a battery during the extended time period.

251. (new): The electronic access control device of claim 248, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the access control device.

252. (new): The electronic access control device of claim 248, wherein the input code or the serial number communicated between the first processor and second processor is encrypted.

253. (new): The electronic access control device of claim 248, wherein a processor is programmed to transmit a serial number stored in a memory through the communication port while the processor is enabled to a device remote to the electronic access control device, and the processor is disabled sometime thereafter.

254. (new): The electronic access control device of claim 253, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the access control device.

255. (new): The electronic access control device of claim 254, wherein the input code or the serial number communicated between the first processor and second processor is encrypted.

256. (new): The apparatus of claim 44, wherein a memory contains a value separate from the access code for limiting access of the apparatus.

257. (new): The apparatus of claim 44, wherein the circuit draws less than 100 micro-amps from a battery during a disabled time period and draws greater than 100 micro-amps from a battery during an enabled time period.

258. (new): The apparatus of claim 44, wherein a time and/or date value is stored in a memory of the device and communicated with a device external to the apparatus.

259. (new): The apparatus of claim 44, wherein the input code or the serial number communicated by a processor is encrypted.

260. (new): The apparatus of claim 256, wherein a processor is programmed to transmit a serial number stored in a memory through the communication port while the processor is enabled to a device remote to the apparatus, and the processor is disabled sometime thereafter.

261. (new): The apparatus of claim 260, wherein a time and/or date value is stored in a memory of the apparatus and communicated with a device external to the apparatus.

262. (new): The apparatus of claim 261, wherein the input code or the serial number communicated by a processor is encrypted.

263. (new): The access control system of claim 248, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

264. (new): The access control system of claim 44, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

265. (new): The access control system of claim 46, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

266. (new): The access control system of claim 53, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

267. (new): The access control system of claim 62, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

268. (new): The access control system of claim 227, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery

while the microprocessor is enabled.

269. (new): The access control system of claim 43, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

270. (new): The access control system of claim 52, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

271. (new): The access control system of claim 61, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

272. (new): The access control system of claim 236, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.

273. (new): The access control system of claim 254, further comprising a low-battery detection circuit for measuring a battery voltage, and wherein the low-battery detection circuit is occasionally disabled and being initiated for measuring the voltage associated with a battery while the microprocessor is enabled.